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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,692	03/18/2004	S. Brandon Keller	200311736-1	6179

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EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,692	KELLER ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication on 03/18/2004. Application 10/803,692 has been examined. In the examination of 10/803,692, claims 1-21 are pending.

Specification

2. The disclosure is objected to because of the following informalities: Applicants are required to provide an updated application status on pending applications (i.e., U.S. Patent Application Serial Numbers need to be stated and U.S. Patent Numbers need to be stated).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-21 are rejected under 35 U.S.C. 102(b)** as being anticipated by Gilbertson (US Patent No. 6,510,405).

As per **claim 1**, Gilbertson discloses a method for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the method comprising:

responsive to a determination that a value of logic level of a signal can be inferred (Fig. 1, #18; col. 6, line 54 to col. 7, line 7; col. 7, line 62-64);

responsive to an attempt by the analysis tool to set the logic level of the signal to a calculated value, determining whether the calculated value is equal to the inferred value (Fig. 5, #98; col. 9, line 56-66); and

if the calculated value is equal to the inferred value, setting the logic level of the signal to the inferred value (col. 3, line 66 to col. 4, line 9; col. 4, line 13-28; col. 6, line 54 to col. 7, line 7; Fig. 5; col. 9, line 56 to col. 10, line 5).

As per **claim 2**, Gilbertson discloses the method of claim 1 further comprising:

the calculated value not equal to the inferred value, preventing the analysis tool from setting a logic level of the signal (Fig. 5; col. 10, line 1-3).

As per **claim 3**, Gilbertson discloses the method of claim further comprising, responsive to preventing, generating an error message indicating that a logic level of the signal has not been set (col. 7, line 29-35; col. 10, line 1-3).

As per **claim 4**, Gilbertson discloses the method of claim 1 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto (Fig. 5, #96; col. 9, line 62-64).

As per **claim 5**, Gilbertson discloses a method for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the method comprising:

responsive to a determination that a value of logic level of a signal can be inferred (Fig. 1, #18; col. 6, line 54 to col. 7, line 7; col. 7, line 62-64);

responsive to an attempt by the analysis tool to set the logic level of the signal to a calculated value, determining whether the calculated value is equal to the inferred value (Fig. 5, #98; col. 9, line 56-66);

if the calculated value is equal to the inferred value, setting the logic level of the signal to the inferred value (col. 3, line 66 to col. 4, line 9; col. 4, line 13-28; col. 6, line 54 to col. 7, line 7; Fig. 5; col. 9, line 56 to col. 10, line 5); and

if the calculated value is not equal to the inferred value, refraining from setting a logic level of the signal (Fig. 5; col. 10, line 1-3).

As per **claim 6**, Gilbertson discloses the method of claim 5 further comprising, responsive to the refraining, generating an error message, wherein the error message indicates that a logic level of the signal has not been set (col. 7, line 29-35; col. 10, line 1-3).

As per **claim 7**, Gilbertson discloses the method of claim 5 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto (Fig. 5, #96; col. 9, line 62-64).

As per **claim 8**, Gilbertson discloses a circuit analysis tool (col. 5, line 63-65; Fig. 1; col. 6, line 7-13; Fig. 2; col. 7, line 54-57) for optimizing relationships between logic commands defining a circuit design input to the tool, the tool comprising:

means responsive to a determination that a value of logic level of a signal can be inferred (Fig. 1, #18; col. 6, line 54 to col. 7, line 7; col. 7, line 62-64) and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for

determining whether the calculated value is equal to the inferred value (Fig. 5, #98; col. 9, line 56-66); and

means responsive to the calculated value being equal to the inferred value for setting the logic level of the signal to the inferred value (col. 3, line 66 to col. 4, line 9; col. 4, line 13-28; col. 6, line 54 to col. 7, line 7; Fig. 5; col. 9, line 56 to col. 10, line 5).

As per **claim 9**, Gilbertson discloses the tool of claim 8 further comprising:

means responsive to the calculated value not being equal the inferred value for preventing the analysis tool from setting a logic level of the signal (Fig. 5; col. 10, line 1-3).

As per **claim 10**, Gilbertson discloses the tool of claim 9 further comprising means responsive to the means for preventing for generating an error message indicating that a logic level of the signal has not been set (col. 7, line 29-35; col. 10, line 1-3).

As per **claim 11**, Gilbertson discloses the tool of claim 8 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto (Fig. 5, #96; col. 9, line 62-64).

As per **claim 12**, Gilbertson discloses a circuit analysis tool for optimizing relationships between logic commands defining a circuit design input to the tool, the tool comprising:

means responsive to a determination that a value of logic level of a signal can be inferred (Fig. 1, #18; col. 6, line 54 to col. 7, line 7; col. 7, line 62-64) and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for

determining whether the calculated value is equal to the inferred value (Fig. 5, #98; col. 9, line 56-66);

means responsive to the calculated value being equal to the inferred value for setting the logic level of the signal the inferred value (col. 3, line 66 to col. 4, line 9; col. 4, line 13-28; col. 6, line 54 to col. 7, line 7; Fig: 5; col. 9, line 56 to col. 10, line 5); and

means responsive to the calculated value not being equal to the inferred value for refraining from setting a logic level of the signal (Fig. 5; col. 10, line 1-3).

As per **claim 13**, Gilbertson discloses the tool claim 12 further comprising means responsive the means for refraining for generating an error message indicating that a logic level of the signal has not been set (col. 7, line 29-35; col. 10, line 1-3).

As per **claim 14**, Gilbertson discloses the tool of claim 12 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto (Fig. 5, #96; col. 9, line 62-64).

As per **claim 15**, Gilbertson discloses a computer-readable medium (col. 4, line 29-47) operable with a computer for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the medium having stored thereon:

computer-executable instructions responsive a determination that a value of logic level of a signal can be inferred (Fig. 1, #18; col. 6, line 54 to col. 7, line 7; col. 7, line 62-64) and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for determining whether the calculated value is equal to the inferred value (Fig. 5, #98; col. 9, line 56-66); and

computer-executable instructions responsive to the calculated value being equal to inferred value for setting the logic level of the signal to the inferred value (col. 3, line 66 to col. 4, line 9; col. 4, line 13-28; col. 6, line 54 to col. 7, line 7; Fig. 5; col. 9, line 56 to col. 10, line 5).

As per **claim 16**, Gilbertson discloses the medium of claim 15 further having stored thereon:

computer-executable instructions responsive to the calculated value not being equal to the inferred value for preventing the analysis tool from setting a logic level of the signal (Fig. 5; col. 10, line 1-3).

As per **claim 17**, Gilbertson discloses the medium of claim 16 further having stored thereon computer-executable instructions responsive to the preventing for returning an error message indicating that a logic level of the signal has not been set (col. 7, line 29-35; col. 10, line 1-3).

As per **claim 18**, Gilbertson discloses the medium of claim 15 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto (Fig. 5, #96; col. 9, line 62-64).

As per **claim 19**, Gilbertson discloses a computer-readable medium operable with a computer for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the medium having stored thereon:

computer-executable instructions responsive a determination that a value of logic level of a signal can be inferred (Fig. 1, #18; col. 6, line 54 to col. 7, line 7; col. 7, line 62-64) and to an attempt by the analysis tool to set the logic level of signal a calculated

value for determining whether the calculated value is equal to the inferred value (Fig. 5, #98; col. 9, line 56-66);

computer-executable instructions responsive the calculated value being equal to the inferred value for setting the logic level of the signal to the inferred value (col. 3, line 66 to col. 4, line 9; col. 4, line 13-28; col. 6, line 54 to col. 7, line 7; Fig. 5; col. 9, line 56 to col. 10, line 5); and

computer-executable instructions responsive the calculated value not being equal to the inferred value for refraining from setting a logic level of the signal (Fig. 5; col. 10, line 1-3).

As per **claim 20**, Gilbertson discloses the medium claim 19 further having stored thereon computer-executable instructions responsive to the refraining for generating an error message, wherein the error message indicates that a logic level of the signal has not been set (col. 7, line 29-35; col. 10, line 1-3).

As per **claim 21**, Gilbertson discloses the medium of claim 19 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto (Fig. 5, #96; col. 9, line 62-64).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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